REMARKS

This is a full and timely response to the final Office action mailed March 4, 2005. Reexamination and reconsideration in view of the foregoing amendments and following remarks is respectfully solicited.

Claims 1-24 are now pending in this application, with Claims 1, 13, and 24 being the independent claims. Claims 1, 3, 5, 13, 16, and 24 have been cosmetically amended herein to even further clarify what is being claimed, and Claims 25-53 were previously canceled without prejudice or disclaimer of the subject matter, these latter claims having been withdrawn from consideration as being drawn to non-elected inventions. No new matter is believed to have been added.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 1-24 were rejected under 35 U.S.C. § 112, second paragraph as allegedly being indefinite. In particular, the Office action alleges that it is unclear how two method steps, namely, testing a simulated model using simulation test vectors and translating the simulation test vectors into device level test vectors, can be performed at the same time. The Office action further alleges that "Applicant's claimed invention shows a testing step 206 for testing a simulated model of the programmed PLD, and following, a translating step 212 for translating at least one simulation test vector into at least one device level test vector, Figure 2." Office action at pp. 2-3.

In response, Applicant points out that the as-filed description clearly supports and describes the claimed feature of "translating at least one simulation test vector into at least one device level test vector while testing the simulated model of the programmed PLD." In particular, Applicant's disclosure at least on page 7, ll. 19-24, indicates this functionality. Moreover, Applicant's disclosure from page 7, l. 19 through page 9, l. 19, and FIG. 6, fully discloses and enables this claim feature. As described therein, the simulation test vectors are translated into device level test vectors while the simulated model of the programmed PLD is being tested.

In further response, Applicant notes that the Office action appears to erroneously allege that the claimed invention is limited to what is explicitly depicted in as-filed FIG.

2. Of course, it is well-settled that an applicant can claim any invention that is fully described and enabled, so long as it is not inconsistent with the disclosure, and is not limited to particular disclosed embodiments. Moreover, unless there is evidence to the contrary, the invention set forth in the claims must be presumed to be that which applicants regard as their invention. In re Moore, 439 F.2d 1232, 169 USPQ 236 (CCPA 1971). Here, there is no evidence to the contrary. Indeed, as Applicant has pointed out, the intrinsic evidence within the as-filed specification fully supports the claimed invention.

In view of the foregoing, reconsideration and withdrawal of the § 112, second paragraph rejection is respectfully solicited.

Rejections Under 35 U.S.C. § 102

Claims 1-7, 13-18, and 24 were once again rejected under 35 U.S.C. § 102 as allegedly being anticipated by U.S. Patent No. 6,021,271 (Winter et al.). This rejection is respectfully traversed.

Independent Claims 1, 13, and 24 each relate to a method of verifying proper design and operation of a programmed programmable logic device (PLD) utilizing a PLD test device. The method defined by each of these independent claims includes developing at least one simulation test vector using a PLD design automation software tool, and testing a simulated model of the programmed PLD using each of the simulation test vectors, and each of these claims recites, *inter alia*, translating at least one simulation test vector into at least one device level test vector while testing the simulated model of the programmed PLD, each device level test vector being in a format readable by the PLD test device.

Winter et al. relates to a method of verifying an electronic circuit design and discloses generating and processing a simulation input file that is used to test the circuit design, and generating a model file of the electronic design. A simulation program is then run using the processed simulation input file and the model file to generate a simulation results file. The simulation results file includes simulation test vectors and

comment lines. When the simulation is completed, the simulation results file is reviewed to confirm the simulation was successful.

Once the simulation results file is reviewed, a test input file is generated by translating the simulation results file to a language used by a test machine. The test input file is then compiled by the tester, and is used to test actual circuits. The test input file generates test vectors in a test results file, which is then compared to corresponding test vectors in the simulation results file.

The Office action alleges that simulation test vectors are translated into device level test vectors as part of step 102 that is depicted in FIG. 2 of Winter et al. More specifically, the Office action alleges, at pages 7 and 8, that the object code that is generated during step 102 is readable by the PLD test device. This, however, is not at all what is disclosed in Winter et al. Rather, what is disclosed is that "[t]he simulation input file is processed to generate object code, an entry table, and a comment table." See col. 4, ll. 13-15. Moreover, Winter et al. clearly states that the simulation program is run on a machine including a computer, data processor, or the like. Nowhere, does Winter et al. disclose, or even remotely suggest, that simulation test vectors are translated into device level test vectors that are in a format readable by the PLD test device as part of step 102. Indeed, it is not until step 122 that Winter et al. even mentions translation of the simulation results file to a language that is usable by a tester. See col. 7, ll. 46-54; FIG. 2. This step occurs after a simulation test is run using the object code that is generated by processing the simulation input file, and after the simulation results file has been reviewed in step 108.

Hence, it is clear that Winter et al. fails to disclose (or even remotely suggest) at least the above-noted feature recited in independent Claims 1, 13, and 24. Namely, Winter et al. fails to disclose translating at least one simulation test vector into at least one device level test vector while testing the simulated model of the programmed PLD. Indeed, Winter et al. explicitly discloses generating a test input file only after the simulation results file has been reviewed.

In view of the foregoing, reconsideration and withdrawal of the § 102 rejection is respectfully solicited.

Rejections Under 35 U.S.C. § 103

Claims 8 and 19 were rejected under 35 U.S.C. § 103 as allegedly being unpatentable over Winter et al., and Claims 9-12, and 20-23 were rejected under 35 U.S.C. § 103 as allegedly being unpatentable over Winter et al. and U.S. Patent No. 6,178,541 (Joly et al.) These rejections are respectfully traversed.

As was noted above, Winter et al. fails to disclose, or even remotely suggest, translating at least one simulation test vector into at least one device level test vector while testing the simulation test model. Moreover, Winter et al. explicitly teaches away from including such a feature, by teaching that a test input file is generated only after the simulation results file has been reviewed.

Joly et al. relates to a method of implementing integrated circuits using an iterative design process. However, this citation is not understood to make up for at least the above-noted deficiency of Winter et al.

Hence, Applicants respectfully request reconsideration and withdrawal of each of the § 103 rejections.

Conclusion

Based on the above, independent Claims 1, 13, and 24 are patentable over the citations of record. The dependent claims are also submitted to be patentable for the reasons given above with respect to the independent claims and because each recite features which are patentable in its own right. Individual consideration of the dependent claims is respectfully solicited.

The other art of record is also not understood to disclose or suggest the inventive concept of the present invention as defined by the claims.

Hence, Applicant submits that the present application is in condition for allowance. Favorable reconsideration and withdrawal of the objections and rejections set forth in the above-noted Office Action, and an early Notice of Allowance are requested.

This Amendment Pursuant to 37 C.F.R. § 1.116 is an earnest attempt to advance prosecution and reduce the number of issues, and is believed to clearly place this

application in condition for allowance. This amendment was not earlier presented because Applicant earnestly believed the prior amendment placed the subjection application in condition for allowance. Accordingly, entry of this amendment is respectfully requested.

Moreover, entry and consideration of this amendment are proper under 37 C.F.R. § 1.116 for at least the following reasons. The amendment overcomes all of the rejections set forth in the above-noted Office action. The amendment does not raise new issues requiring further search or consideration. Additionally, the present amendment places the application in better form for appeal, which Applicant fully intends to pursue, if necessary. Therefore, entry and consideration of the present amendment are proper under 37 C.F.R. § 1.116 and are hereby requested.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone the undersigned attorney at the below-listed number.

If for some reason Applicant has not paid a sufficient fee for this response, please consider this as authorization to charge Ingrassia, Fisher & Lorenz, Deposit Account No. 50-2091 for any fee which may be due.

Respectfully submitted,

INGRASSIA FISHER & LORENZ

Dated: 5/2/05

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